

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

- BLDC Motor driver
- DC-DC
- Load switch

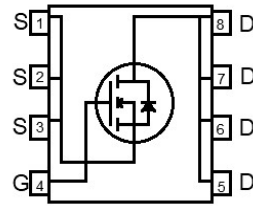
• Ordering Information:

Part NO.	ZMSA012N06NC
Marking	ZMS012N06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

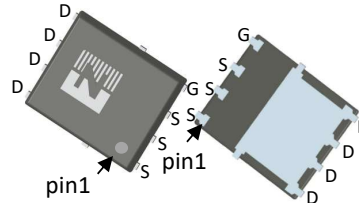
• Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage ^①	V_{GS}		±20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	223	A
	I_D	$T_C=75^\circ\text{C}$	182	A
	I_D	$T_C=100^\circ\text{C}$	158	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	669	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	167	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.3	W
Operating Junction Temperature	T_J		-55 to +175	°C
Storage Temperature	T_{STG}		-55 to +175	°C
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	320	mJ
		L=0.5mH, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	680	mJ
ESD Level (HBM)	CLASS 2			

• Product Summary



$V_{DS} = 60\text{V}$
 $R_{DS(ON)} = 1.2\text{m}\Omega$
 $I_D = 223\text{A}$



DFN5*6



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.9	$^{\circ}C/W$
Thermal resistance, junction-ambient	$R_{thJA}^{\textcircled{2}}$		-	45	$^{\circ}C/W$
Soldering temperature	T_{sold}		-	260	$^{\circ}C$

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.6	1.9	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS} = 0V, V_{DS} = 60V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 40A$		1.2	1.6	m Ω
		$V_{GS} = 4.5V, I_D = 30A$		1.8	2.3	
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_{SD} = 10A$		30		S
Diode Forward Voltage	V_{FSD}	$V_{GS} = 0V, I_{SD} = 40A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f = 1MHz, V_{DS} = 25V$	-	4770	-	pF
Output capacitance	C_{oss}		-	1880	-	
Reverse transfer capacitance	C_{rss}		-	81	-	
Gate Resistance	R_g	$f = 1MHz$	-	1.6		Ω
Total gate charge	Q_g	$V_{DD} = 15V, I_D = 20A, V_{GS} = 10V$	-	65	-	nC
Gate - Source charge	Q_{gs}		-	13	-	
Gate - Drain charge	Q_{gd}		-	9	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS} = 10V, V_{DS} = 15V, R_G = 3.3\Omega, I_D = 20A$	-	15	-	ns
Turn-ON Rise time	t_r		-	10	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	26	-	ns
Turn-Off Fall time	t_f		-	17	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD} = 20V, di_S/dt = 100A/\mu s, I_S = 50A$	-	48	-	ns
Reverse Recovery Charge	Q_{RR}		-	47	-	nC

Fig.1 Gate-Charge Characteristics

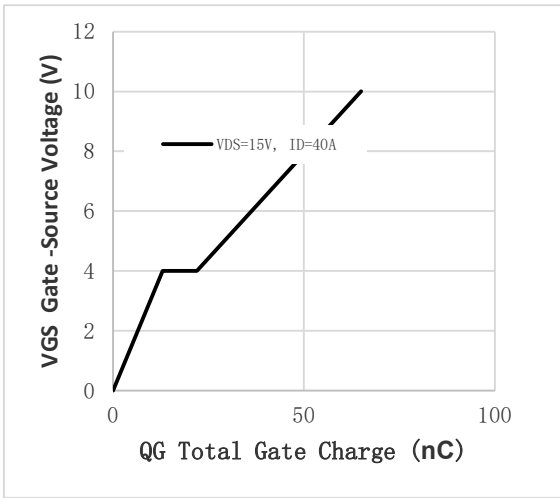


Fig.2 Capacitance Characteristics

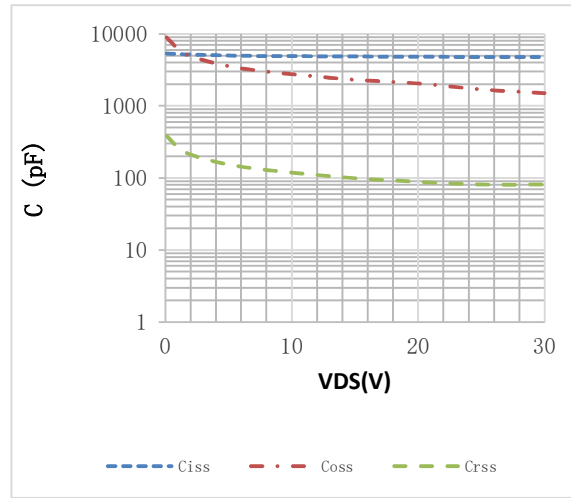


Fig.3 Power Dissipation

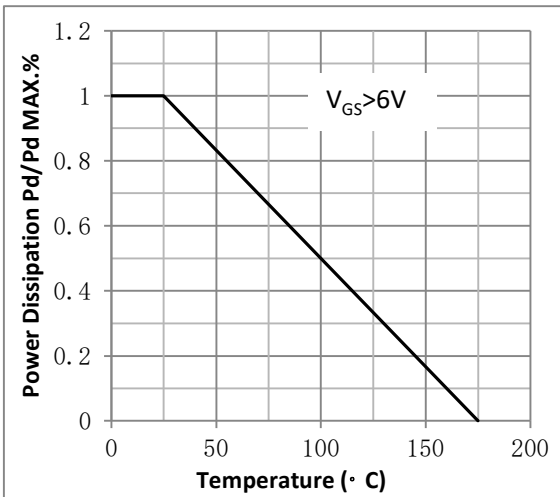


Fig.4 Typical output Characteristics

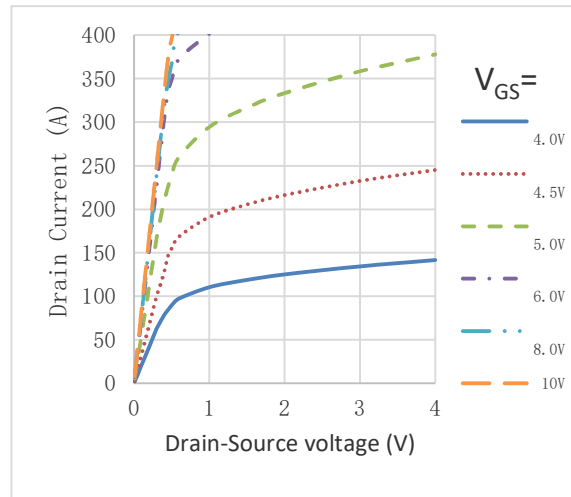


Fig.5 Threshold Voltage V.S Junction Temperature

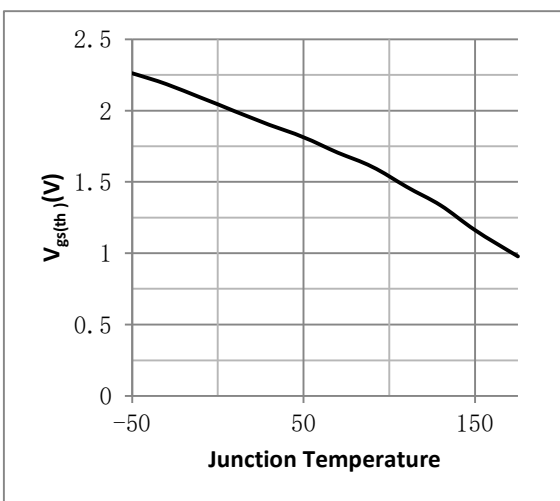


Fig.6 Resistance V.S Drain Current

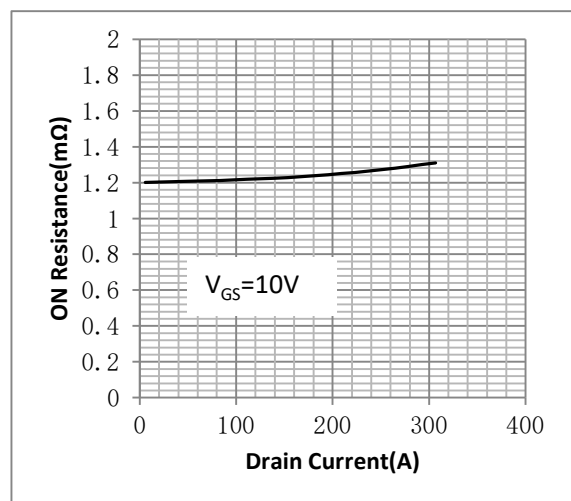


Fig.7 On-Resistance VS Gate Source Voltage

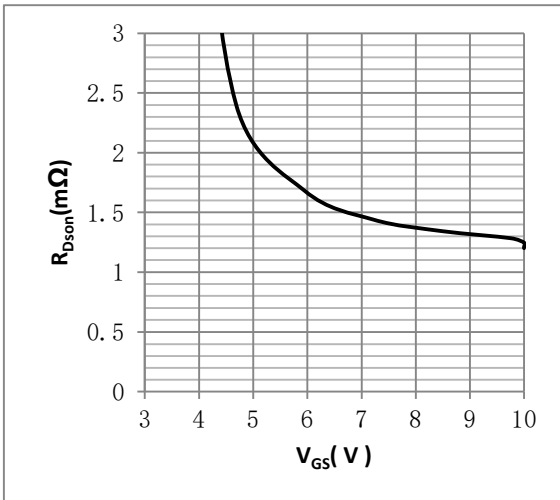


Fig.8 On-Resistance V.S Junction Temperature

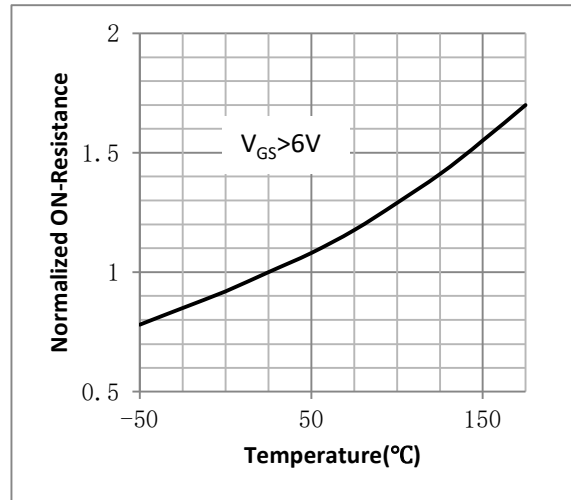


Figure 9. Diode Forward Voltage vs. Current

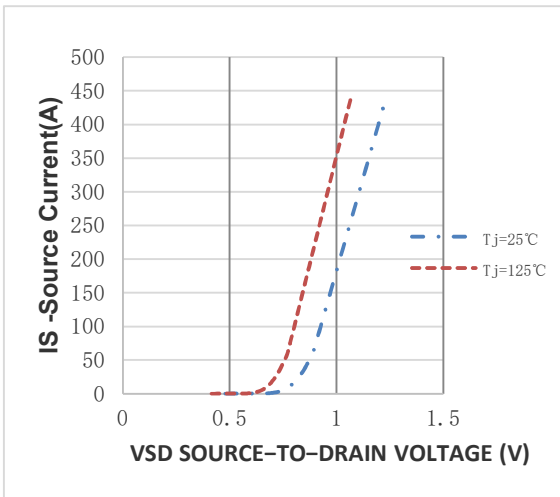


Figure 10. Transfer Characteristics

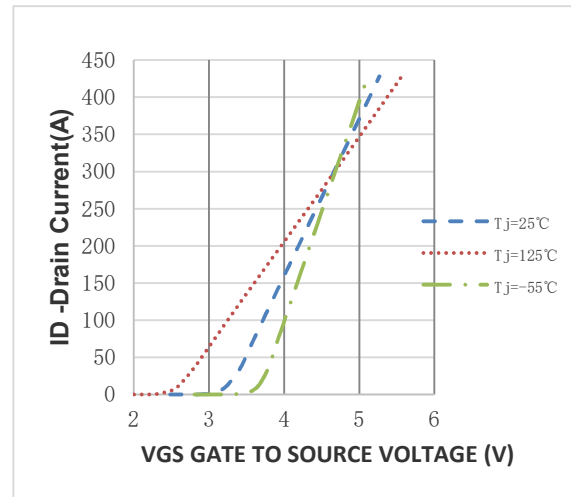


Fig.11 Safe Operating Area

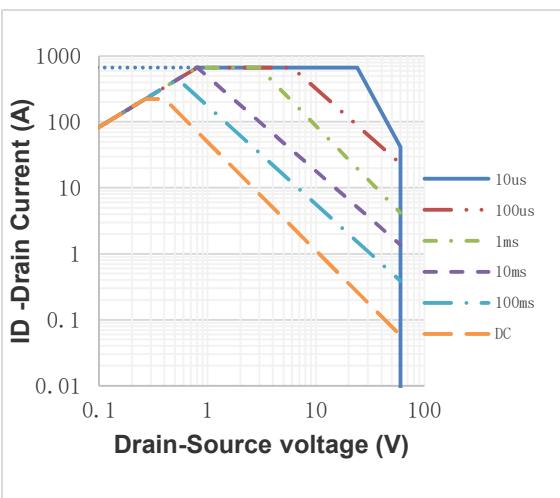
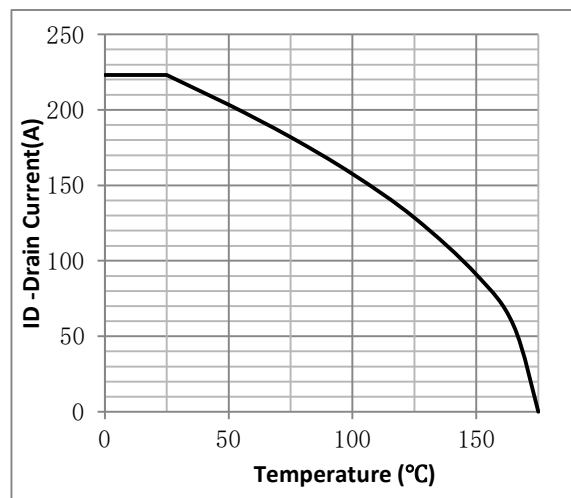
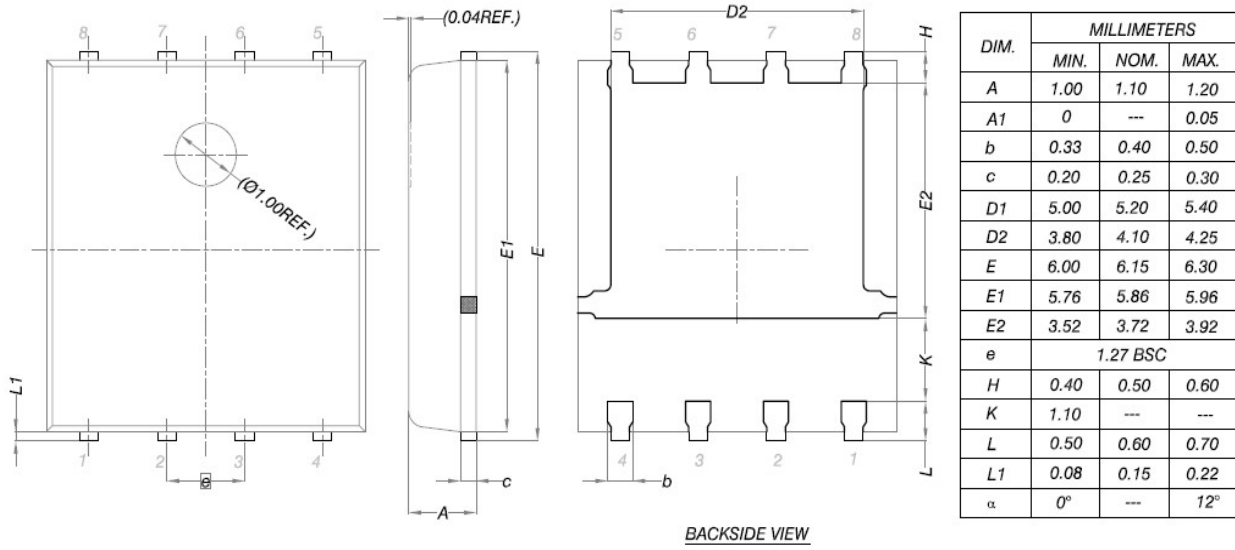


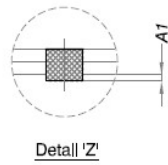
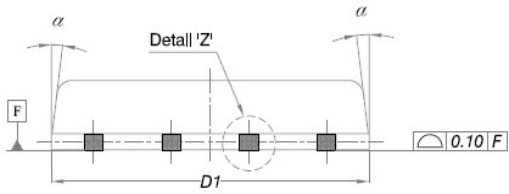
Fig.12 ID vs. Junction Temperature^③



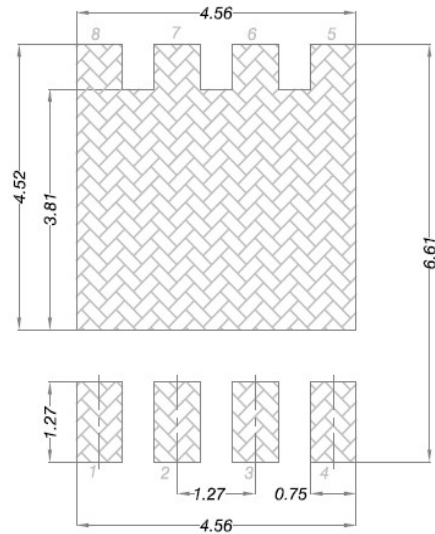
•DFN5*6 Package Outline



BACKSIDE VIEW



Land Pattern
(Only for Reference)



Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature.
 $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2022.12.15	
B	2023.2.20	1.Add Dynamic characteristic t_f , t_r etc.
C	2023.10.12	Modify R_{thjc} , $R_{dson@4.5v}$
D	2023.12.4	Correct BVDS
E	2024.5.20	Correct C_{iss} , Q_g
F	2026.1.28	Update POD